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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,773	10/29/2003	Hung-Yi Kuo	JCLA10908	8873

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EXAMINER	
STIGLIC, RYAN M	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,773	KUO, HUNG-YI	
	Examiner	Art Unit	
	Ryan M. Stiglic	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 and 3-18 are pending and have been examined.

2. Claims 1 and 3-18 are rejected.

Response to Arguments

3. Applicant's arguments, see pages 8-9, filed March 8, 2006, with respect to the rejection(s) of claim(s) 1, 2, 5-6, 8, 11, 12 and 14-17 under 35 U.S.C. §103(a) as being unpatentable over the PCI to PCI Bridge Architecture Specification in view of Okazawa have been fully considered and are moot in view of the Examiner's application of a new ground(s) of rejection is made in view of Tanaka et al. (U.S. 5,933,613).

4. Applicant's arguments, see pages 9-10, filed March 8, 2006, with respect to the rejection of claims 1-2, 4-8 and 10-18 under 35 U.S.C. §103(a) as being unpatentable over Klein and PCI bridge have been fully considered and are persuasive. The rejection of the claims has been withdrawn.

5. The rejection of claims 8-13 under 35 U.S.C. §112, second paragraph, have been withdrawn in light of applicant's amendments.

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1, 5-6, 8, 11-12 and 14-17 rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 5,933,613) in view of Okazawa et al. (US 5,668,956).

Tanaka discloses a bus bridge circuit (Fig. 1 & 3, 40) connected between two peripheral buses (Fig. 1, items 200 and 201). The bridge comprises two control circuits (Fig. 3, items 401 and 403) that decode incoming bus cycles to determine the type of transaction and the destination of the transaction (col. 6, ll. 23-30). Upon receipt of a transaction (from the primary bus 200 for example) the control circuit decodes the signals and categorizes incoming transactions into three possible transaction types: internal I/O transactions (col. 5, line 61- col. 6, line 9; col. 6, ll. 31-36); internal memory transactions (col. 5, line 61- col. 6, line 9; col. 6, ll. 37-44); and external secondary bus transactions (col. 5, line 61- col. 6, line 9; col. 6, ll. 45-62). The external secondary bus transactions are the only transactions Tanaka discloses as being sent to the secondary bus **201** (col. 6, ll. 57-62). As such, it is inherent that the other two transaction types (internal I/O and internal memory) are not reproduced on the second bus because Tanaka does not explicitly disclose gaining access to the secondary bus as they do with respect to external secondary bus transactions (col. 6, ll. 57-62). It is clear from the disclosure of Tanaka that only transaction types destined for the secondary bus are transmitted across the bridge circuit **40**, however Tanaka does not disclose an inhibiting signal for use in prohibiting the retransmission of signals from a primary bus to a secondary bus.

Okazawa teaches a bus bridge (Fig. 1 & 4, 103) used to connect a primary bus (Fig. 1 & 4, 111) and secondary bus (Fig. 1 & 4, 113). Okazawa teaches inhibiting re-transmission of bus cycles onto a secondary bus when the destination of the bus cycle is not the secondary bus. Instead of re-transmitting the bus cycle to all downstream buses (Fig. 1 & 4, 111, 112, and 113), the bus

cycle is only re-transmitted to the proper destination bus (col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16) by the connection controller (Fig. 4, 401) and the data path switch (Fig. 4, 402). The connection controller **401** receives bus cycles from the connected buses and decodes bus cycles to output an indicator signal (code information outputted from the sequencer 613 of Fig. 6). The indicator signal is further decoded into a plurality of inhibiting signals (Fig. 5, 511-513; and Fig. 6, 618-621) that inhibit the re-transmission of bus cycles on a subordinate bus.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the bus cycle inhibiting circuit of Okazawa into the bridge circuit of Tanaka such that maximization of the utilization efficiency of buses connected to the control chip/bridge is achieved (Okazawa, col. 11, line 64- col. 12, line 4).

For claims 1, 14 and 16 Tanaka in view of Okazawa teaches:
A control chip (Tanaka; Fig. 1, 40; Okazawa; Fig. 1, 103) with a bus cycle inhibiting function for preventing internal bus cycle type of the control chip, picked up from a first bus, from being re-transmitting to a second bus, the first bus and the second bus both coupled to the control chip, the control chip comprising:

- a bus cycle inhibiting circuit (Tanaka; Fig. 3, 401 and 403; Okazawa; Fig. 6, 613) for receiving a bus cycle from the first bus and outputting an inhibiting signal (Okazawa; Fig. 5, 511-513 and Fig. 6, 618-621) once the bus cycle is determined to be an internal bus cycle type of the control chip (Tanaka; col. 5, line 54 – col. 6, line 62; Okazawa; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16) the bus cycle inhibiting circuit comprising;

- a bus resource decode circuit for receiving a bus cycle from the first bus and outputting an indicator signal representing the particular type of bus cycle when the bus cycle is determined to be an internal bus cycle type of the control chip (Tanaka; Fig. 4, items 451 and 452; col. 5, line 54 – col. 6, line 62; Okazawa; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16; Fig. 6, 609-610), the bus resource decode circuit comprising;
  - an input/output resource decode unit (Tanaka; Fig. 4, 453; col. 5, line 54 – col. 6, line 62) for receiving the bus cycle from the first bus and outputting the indicator signal representing an internal input/output bus cycle when the bus cycle is determined to be an internal input/output bus cycle (Okazawa; Fig. 5, 511-513 and Fig. 6, 618-621); and
  - a logic circuit for outputting the inhibiting signal according to a preset enable value (Okazawa; Fig. 6, 607-608 are registers/latches that store control signals from each of the processor and system buses (col. 8, ll. 19-34). Here the control signals represent the present/state of the respective bus, therefore the control signals stored in the latches act as enable signals) and the indicator signal (Okazawa; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16; Fig. 6, 614; Fig. 5, 510); and

- a bus bridging circuit coupled to the bus cycle inhibiting circuit for inhibiting the re-transmission of the bus cycle on receiving the inhibiting signal (Okazawa; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16).

For claims 5 and 11 Tanaka in view of Okazawa teaches:

The control chip of claim 1, wherein the preset enable value is stored inside a register (Okazawa; col. 8, ll. 19-34; Fig. 6, 607-608).

For claims 6, 12 and 17 Tanaka in view of Okazawa teaches:

The control chip of claim 1, wherein the second bus comprises a peripheral component interconnect (PCI) bus (Tanaka; col. 5, line 54 – col. 6, line 62).

For claim 8 Tanaka in view of Okazawa teaches:

A bus cycle inhibiting circuit for a control chip having at least a first bus and a second bus, comprising:

- a bus resource decode circuit for receiving a bus cycle from the first bus (Okazawa; Fig. 6, 613; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16) and outputting an indicator signal (Fig. 6, Code Information from 613) representing the particular type of bus cycle when the bus cycle is determined to be an internal bus cycle the bus resource decode circuit comprising:
    - an input/output resource decode unit (Tanaka; Fig. 4, 453; col. 5, line 54 – col. 6, line 62) for receiving the bus cycle from the first bus and outputting the indicator signal representing an internal input/output bus cycle when the bus cycle is determined to be an internal input/output bus cycle (Okazawa; Fig. 5, 511-513 and Fig. 6, 618-621); and

- a logic circuit (Okazawa; Fig. 6, 614; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16) for outputting the inhibiting signal (Okazawa; Fig. 6, 618-621) according to a preset enable value (Okazawa; Fig. 6, 607-608 are registers/latches that store control signals from each of the processor and system buses (col. 8, ll. 19-34). Here the control signals represent the present/state of the respective bus, therefore the control signals stored in the latches act as enable signals) and the indicator signal (Okazawa; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16).

For claim 15 Tanaka in view of Okazawa teaches:

The bus cycle inhibiting method of claim 14, wherein the inhibiting signal is issued when the bus cycle is found to be an internal input/output bus cycle, an internal memory bus cycle or an internal configuration bus cycle (Tanaka; col. 5, line 54 – col. 6, line 62).

8. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 5,933,613) in view of Okazawa et al. (US 5,668,956) as applied to claim 1 above and further in view of PCI to PCI Bridge Architecture Specification.

As previously discussed above, Tanaka in view of Okazawa teach a PCI-to-PCI bus bridge circuit coupled between two buses. The bus bridge comprises a bus cycle inhibiting circuit for receiving a bus cycle from the first bus and outputting an inhibiting signal once the bus cycle is determined to be an internal bus cycle. The bus cycle inhibiting circuit of Tanaka in view of

Okazawa is comprised of a bus resource decode circuit for receiving the bus cycle from the first bus and outputting an inhibit signal and a logic circuit for outputting the inhibiting signal according to a present enable value and the indicator signal. An input/output resource decode unit (Tanaka; Fig. 4, 453; col. 5, line 54 – col. 6, line 62) for receiving the bus cycle from the first bus and outputting the indicator signal (Okazawa; Fig. 6, 609-610; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16) representing an internal input/output bus cycle (Tanaka; col. 6, ll. 31-36) when the bus cycle is determined to be an internal input/output bus cycle is found in the bus resource decode circuit. The bus resource decode circuit also includes a memory resource decode unit (Tanaka; Fig. 4, 454; col. 5, line 54 – col. 6, line 62) for receiving a bus cycle from the first bus and outputting an indicator signal (Okazawa; Fig. 6, 609-610; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16) representing an internal memory bus cycle (Tanaka; col. 6, ll. 37-43) when the bus cycle is determined to be an internal memory bus cycle. The bus resource decode circuit of Tanaka in view of Okazawa however fails to explicitly teach type-0 configuration commands used in PCI-to-PCI bus bridges to define characteristics of the bus bridge relevant to its functionality.

The PCI to PCI Bridge Architecture Specification (hereinafter PCI Bridge) discloses a bridge (Fig. 1-2, page 13) that connects two PCI buses. A set of configuration registers within the bridge contains information relevant to the functionality of the bridge. In order for a processor of the computer system to have access to the configuration registers a configuration transaction (cycle) must be initiated on the primary bus (where the primary bus is the upstream bus). The configuration transaction is summarized by two types of transactions, a type 0 configuration

transaction and a type 1 configuration transaction. Type 1 configuration transactions are configuration cycles that are destined for a device/bridge not residing on the primary bus. In other words, if a type 1 configuration command is received by the bridge the type 1 configuration command will be forwarded to a subordinate bus for further processing. In contrast, a type 0 configuration transaction is a configuration cycle that is destined for devices/bridges on the primary bus. "A Type 0 configuration transaction is not forwarded across a bridge but is used to configure a bridge...(page 19)" Therefore the PCI to PCI Bridge Architecture Specification teaches that Type 0 configuration cycles are *inhibited* from re-transmission. While some inherent bus cycle inhibiting circuit and bus bridging circuit means are present, the PCI to PCI Bridge Architecture Specification does not expressly teach the structure of such circuits.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement type-0 configuration commands, a feature inherent to all PCI-to-PCI bus bridges, in the bus bridge of Tanaka in view of Okazawa such that the bus bridge may be configured to meet system requirements.

9. Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 5,933,613) in view of Okazawa et al. (US 5,668,956) as applied to claims 1 and 8 above and further in view of what was well known in the art at the time of applicant's invention.

As previously discussed above, Tanaka in view of Okazawa teach a bus bridge circuit coupled between two buses. The bus bridge comprises a bus cycle inhibiting circuit for receiving a bus cycle from the first bus and outputting an inhibiting signal once the bus cycle is determined to be an internal bus cycle. The bus cycle inhibiting circuit of Tanaka in view of Okazawa is comprised of a bus resource decode circuit for receiving the bus cycle from the first bus and outputting an inhibit signal and a logic circuit for outputting the inhibiting signal according to a present enable value and the indicator signal. Tanaka in view of Okazawa however are silent on the structure of the logic circuit used to output the inhibiting signal according to a present enable value and the indicator signal.

Official Notice is taken that the use of AND gates and OR gates are well known in logic circuits. The AND gates and OR gates represent two of the most fundamental logic circuit components in digital circuitry. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the logic circuit of Tanaka in view of Okazawa with AND gates and OR gates since their use is well known for logic circuitry.

10. Claims 7, 13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view Okazawa as applied to claims 1, 8 and 14 above, and further in view of what was well known at the time of Applicant's invention as evidenced by Gulick (US 5,926,629).

As previously discussed Tanaka in view of Okazawa teach a bridge that inhibits the re-transmission of internal bus cycles received from a primary bus. The bridge comprises a bus

cycle inhibiting circuit for detecting the presence of an internal bus cycle and a bus bridging circuit for inhibiting the re-transmission of the internal bus cycle on a secondary bus. Neither Tanaka nor Okazawa however explicitly teach of the bridge being a well known Southbridge.

Gulick teaches a Southbridge (Fig. 2 & 3, 201) that connects to a Northbridge of the computer system through a primary bus. The Southbridge provides a connection between the system processor(s), via the Northbridge, and a plurality of peripheral buses (i.e. Fig. 3, USB Controller, EIDE Controller, ISA Bus 307). Therefore the Southbridge is solely responsible for increasing the performance of the system by providing interfaces to a plurality of I/O devices and various other peripherals (col. 4, line 63 – col. 6, line 25).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement a Southbridge as the bridge of Tanaka in view of Okazawa such that the system of Tanaka in view of Okazawa is provided with the expansion capabilities of a Southbridge.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

RMS

PAUL R. MYERS
PRIMARY EXAMINER